The new dynamic parameters of CAN SIC

The CiA 601-4 specification for CAN SIC transceivers is released and will be hand over to the updated ISO 11898-2 soon; the CiA 601-1 specification helps to understand the CAN FD high-speed transmission. The dynamic parameters are discussed in this article.

(Source: Adobe Stock)

The main difference between CAN FD transceivers and CAN SIC transceivers is the transmitter. The CAN protocol allows collision on the network. This means two or more nodes can transmit data at the same time. This is needed to support arbitration and error frames. To avoid damages on the transceiver in case of a collision, the transmitter transmits only a dominant signal on the network. The recessive signal is caused by the termination resistors only. In Figure 1 the typical behavior of a CAN FD transceiver is demonstrated.

Phase 1: TxD is logical_1 and the transmitter output stages are high impedant and the network is recessive.

Phase 2: TxD changes to logical_0 and the transmitter output will be switched on. The transmitter impedance changes from high to low impedance. The level on the network is dominated by the transmitting node.

Phase 3: TxD is logical_0 and the transmitter output is switched on. The transmitter impedance is low impedant and dominates the level on the network.

Phase 4: TxD changes to logical_1 and the transmitter output will be switched off. The transmitter becomes high impedant and the level on the network will be controlled by the termination resistors.

Phase 5: TxD is logical_1 and the transmitter output stages are high impedant.
The level on the network is controlled by the termination resistor.

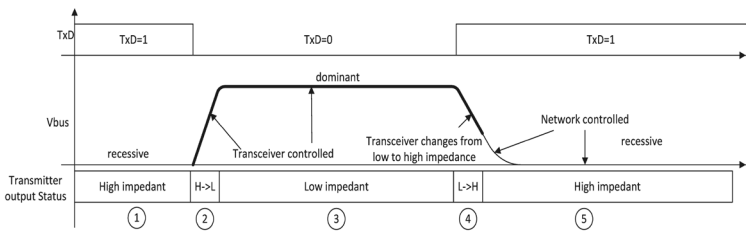

Figure 1: Typical transmitter behavior of a CAN FD transceiver (Source: Infineon)

The main difference between a CAN FD transceiver and CAN SIC transceiver is the transition dominant to recessive. The transition dominant to recessive caused ringing and reflection due to the change from low impedance to high impedance. To reduce this ringing and reflection, the SIC transmitter changes from low impedance state in dominant to a medium impedance state during the transition dominant to recessive and for a limited time afterwards. In Figure 2 the typical behavior of a CAN SIC transceiver is demonstrated.

Phase 1: TxD is logical_1 and the transmitter output stages are high impedant and the network is recessive. The behavior is the same like a CAN FD transceiver.

Phase 2: TxD changes to logical_0 and the transmitter output will be switched on. The transmitter impedance changes from high to low impedance. The network is dominated by the transmitting node. The behavior is the same like a CAN FD transceiver.

Phase 3: TxD is logical_0 and the transmitter output is switched on. The transmitter impedance is low impedant and dominates the level on the network. The behavior is the same like a CAN FD transceiver.

Phase 4: TxD changes to logical_1 and the transmitter output stages are changing from low impedant to a medium dependant state to pull actively the differential signal (V_{CANH} - V_{CANL}) close to 0 V for a limited time (SIC time).

Phase 5: TxD is logical_1 and the transmitter output stages pull for a limited time (called SIC time) the differential signal actively to 0 V with an impedance of around 100 Ω, which is the typical wire impedance of a twisted pair wire. This behavior is different to CAN FD transceiver.

Phase 6: TxD is logical_1 and the transmitter output stages are high impedant.
The level on the network is controlled by the termination resistor. Same behavior like a CAN FD transceiver in Phase 5.

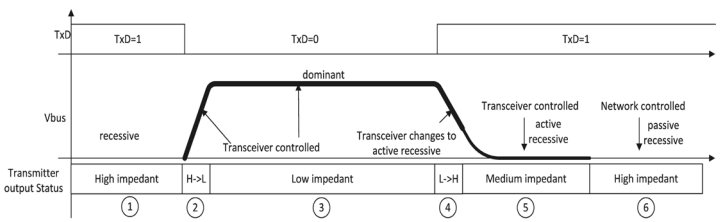

Figure 2: Typical transmitter behavior of a CAN SIC transceiver (Source: Infineon)

The maximum SIC time are 530 ns and this time might be longer than a bit time. Is the bit time shorter than the SIC time, the transmitter changes directly from SIC state into dominant state. This allows bit times which are shorter than the SIC time. The advantage is that for high bit rates one or more recessive bits in a row are supported by the SIC feature. So, ringing effects and reflection effects in a network can be longer than the bit time.

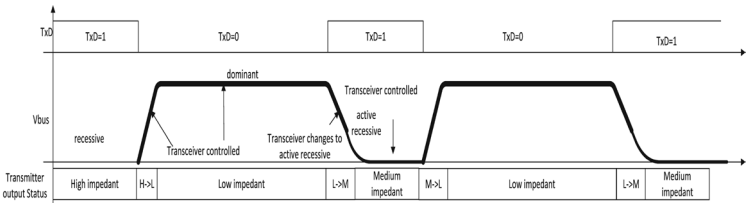

Figure 3: Typical transmitter behavior of a CAN SIC transceiver and high bit rates (Source: Infineon)

Signal improvement time

The signal improvement unit will be activated during the falling edge of the network signal (dominant to recessive transition). At which point exactly depends on the implementation and is difficult to measure. Also, for a network designer this point is not of interest. It is important to know how long the signal improvement capability is active. To make this easy to analyze and measure, the signal improvement time starts with the rising edge of the TxD signal and ends latest after 530 ns. Figure 4 illustrates how the signal improvement time is specified.

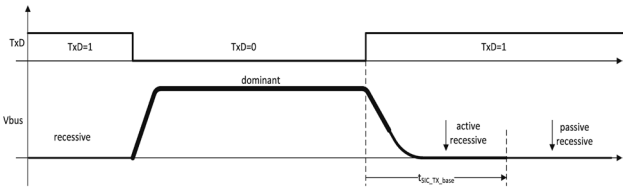

Figure 4: Signal improvement time definition (Source: Infineon)

Loop-delay symmetry

The loop-delay is the time between the TxD input signal and the RxD output signal of a transmitting transceiver. Figure 5 illustrates the transceiver loop-delay.

Figure 6 illustrates, how the loop-delay is specified. The delay of the recessive-to-dominant transition (falling edge in TxD) starts at 30 % of the TxD voltage swing and stops at 30 % of the RxD output level.

The dominant-to-recessive transition (rising edge) starts at 70 % of the TxD level and stops at 70 % of its RxD level. The loop-delay symmetry is from 70 % of a rising edge to 30 % of a falling edge of a recessive bit on RxD. The symmetry called received bit width variation is calculated according to the following formula:

$$t_{\Delta Bit(RxD)} = t_{Bit(RxD)} - t_{nom(TxD)}.$$

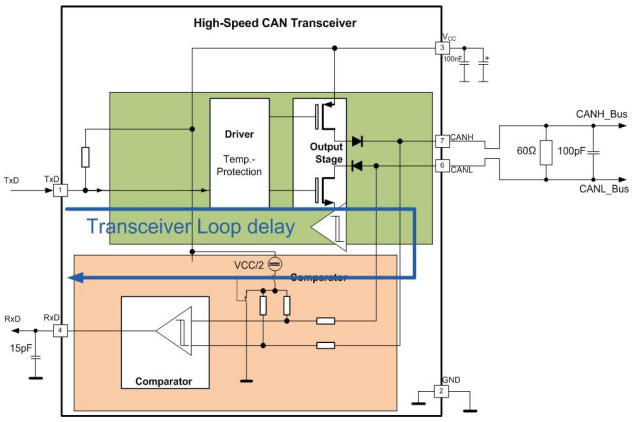

Figure 5: Transceiver loop-delay elements (Source: Infineon)

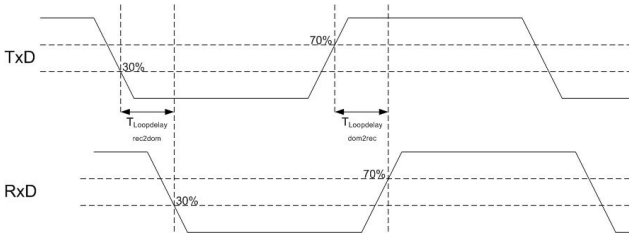

Figure 6: Transceiver loop-delay specification (Source: Infineon)

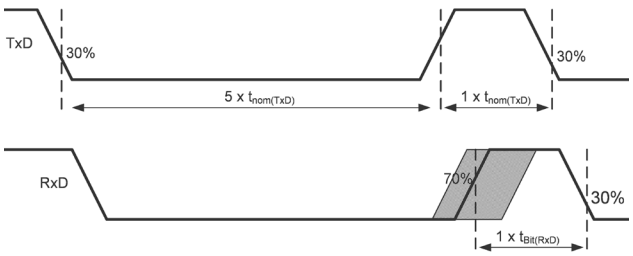

Figure 7: Transceiver loop-delay symmetry specification (Source: Infineon)

Table 1: The TxD to RxD loop-delay and loop delay symmetry parameter

Parameter set	A	B	C
$t_{\Delta Bit(RxD)}$ min	-100 ns	-80 ns	-30 ns
$t_{\Delta Bit(RxD)}$ max	+50 ns	+20 ns	+20 ns
t_{nom}	≥ 500 ns	≥ 200 ns	≥ 125 ns
$t_{(loop\ delay)}$	≤ 255 ns	≤ 255 ns	≤ 190 ns
Busload	60 Ω, 100 pF	60 Ω, 100 pF	60 Ω, 100 pF

Transceiver Tx delay symmetry

The Transceiver Tx delay is the time between the TxD input signal and the differential nework output signal as shown in Figure 8.

The transmitter delay is the time between the rising edge of TxD signal (70 %), to the falling edge of the differential signal on the network (500 mV) or the time between the falling edge of the TxD signal (30 %) and the rising edge of the differential signal of the network. The symmetry is the difference between the recessive-to-dominant delay and the dominant-to-recessive delay. The symmetry is specified like for the transmitter delay. The recessive bit-length is the distance between 500 mV of the falling edge to 900 mV of the rising

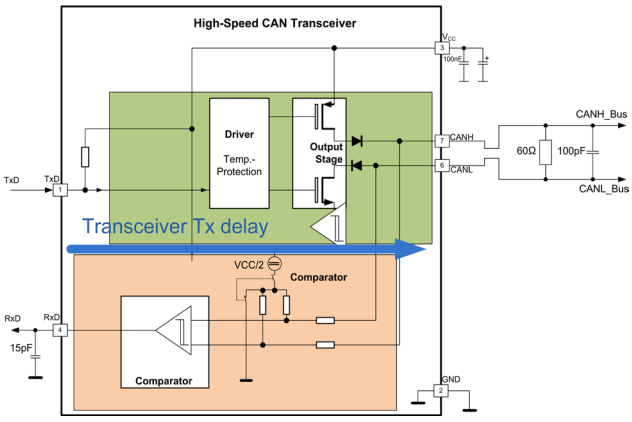

Figure 8: Transceiver Tx delay (Source: Infineon)

edge (see Figure 9). Table 2 shows the tBit(Bus) parameter values. The parameters are now specified as a deviation compared to the nominal bit width of the TxD signal and is valid up to the maximum specified bit rate of the device.

Table 2: Network recessive bit-width (transmitter delay symmetry)

Parameter set	A	B	C
$t_{Bit(Bus)}$ min	-65 ns	-45 ns	-10 ns
$t_{Bit(Bus)}$ max	+30 ns	+10 ns	+10 ns
$t_{prop(TxD-busdom)}$	Not defined	Not defined	80 ns
$t_{prop(TxD-busrec)}$	Not defined	Not defined	80 ns
Busload	60 Ω, 100 pF	60 Ω, 100 pF	60 Ω, 100 pF

In the current ISO 11898-2 specification the parameter Set A, are the parameters for bit rates up to 2 Mbit/s and parameter set B for bit rates up to 5 Mbit/s. The parameter set C is now for SIC transceivers.

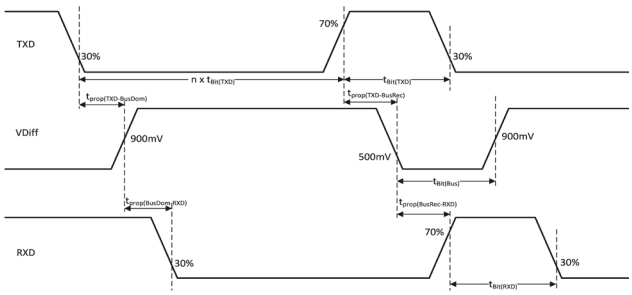

Figure 9: Specification of the transmitter and receiver delay and the bit width variation (Source: Infineon)

Transceiver Rx delay symmetry

The Transceiver Rx delay is the propagation time between the differential network signal and the RxD output signal. The definition is illustrated in Figure 9. This symmetry depends on:

- Production dispersion
- Temperature variation
- Receiver thresholds
- Supply voltage variation
- Network differential voltage (V_{diff}) slew rate

Δt_{Rec} is a calculated as follows:

$$\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Bus)}$$

Table 3: Tolerance of the receiver

Parameter set	A	B	C
$t_{Bit(Bus)}$ min	-65 ns	-45 ns	-20 ns
$t_{Bit(Bus)}$ max	+40 ns	+15 ns	+15 ns
$t_{prop(busdom-RXD)}$	Not defined	Not defined	110 ns
$t_{prop(busrec-RXD)}$	Not defined	Not defined	110 ns
Load on RxD	15 pF	15 pF	15 pF

In Table 3 the limits of the receiver delay and its symmetry for CAN FD transceiver parameter (parameter set A and B) and for SIC transceiver (parameter set C) are shown.

The new SIC feature improves existing networks and makes the communication in these networks more reliable. The more symmetric parameter allows also higher bit rates up to 8 Mbit/s. The SIC transceivers are a big step into the future of CAN and this concept is also used in the new CAN SIC XL transceiver for CAN XL communication. ◀

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