Scalable processors for future software-defined vehicles

NXP has announced the S32N family of vehicle super-integration processors to support the transition to future vehicles. The first family member S32N55 includes a CAN hub with four CAN XL and 24 CAN FD ports.

The S32N family enables automakers to evolve their vehicle electrical/electronic (E/E) architectures and centralize cross-vehicle functions previously implemented as individual hardware boxes (ECUs: electronic control units) into a central compute ECU. The latter can be a central vehicle controller focused on real-time applications or a central vehicle computer that also provides applications processing.

The introduced processors can integrate dozens of cross-vehicle functions with mixed-criticality. The used hardware isolation and virtualization technologies ensure freedom from interference between functions. Supported by complementary system components, software tools, and pre-integrated software, the processors are designed to accelerate software-defined vehicle (SDV) development and reduce vehicle cost and complexity. The processors offer many combinations of safe, real-time, and applications processing cores. This meets central computing needs ranging from real-time operating systems running deterministic vehicle control to high-level operating systems running vehicle management and OEM (original equipment manufacturer) applications and services.

All S32N products integrate a CAN hub, an advanced hardware security engine, and a multi-port TSN Ethernet switch. Some processors also support Ethernet packet acceleration, AI/ML acceleration, and inter-compute PCI Express services.

Core vehicle functionality

Using S32N processors enables automakers to centrally consolidate core vehicle functionality in a central compute ECU. The latter can be custom-built to suit the diverse requirements of vehicles (see Figure 1). In current vehicles, around 40% of the weight is electronics and wiring. Reducing the number and weight of car components enables the automotive industry to offer lighter and more energy-efficient vehicles.

NXP’s S32 Coreride central compute solution is based on S32N processors. The solution combines S32N compute, vehicle networking, and system power management (such as the FS04 safe power management IC) to accelerate central compute development. The solution was designed to adhere to the automotive industry standards for vehicle functional safety (ISO 26262), security (ISO/SAE 21434), and reliability. When combined with software from company’s partner ecosystem, including NXP’s pre-integrated isolation execution environments, NXP will offer the holistic SDV (software defined vehicle) solution that can scale across the vehicle, and vehicle fleets.

First family member: S32N55

NXP released the first S32N55 family member as the heart of the S32 Coreride central compute solution. Former, vehicle propulsion, vehicle dynamics, chassis control, body, and other core vehicle functions have been implemented as discrete electronic control units (ECUs), each with their own micro-controller and wiring. Vehicle functions can now be consolidated into an S32N55 processor with multiple isolation execution environments, which allows to reduce ECU hardware costs. Decreased material and reduced weight also contribute to sustainability and extended driving range. For carmakers, it results in lower manufacturing complexity and time.
With the “core-to-pin” hardware isolation and virtualization technologies, processor’s resources can be dynamically partitioned. Vehicle functions can be managed independently, including fault handling and reset. They can receive independent software updates with the over-the-air (OTA) upgradeability.

The automotive-grade S32N55 processor integrates 16 split-lock Arm Cortex-R52 processor cores running at 1.2 GHz for real-time compute. The cores can operate in split or lockstep mode to support different functional safety levels up to ISO 26262 ASIL D (automotive safety integrity level). Two auxiliary pairs of lockstep Cortex-M7 cores support system and communication management. Tightly-coupled integrated memory and 48 MiB of system SRAM enable fast execution with low-latency accesses. A firewalled Hardware Security Engine provides a root of trust for secure boot, security services, and key management.

An integrated CAN hub for internal routing of 24 CAN FD networks and four CAN XL interfaces, time-sensitive networking (TSN) 2.5-Gbit/s Ethernet switch, a and a PCI Express Gen 4 interface help reduce wiring and system cost. Memory can be expanded with LPDDR4X/5/5X DRAM, LPDDR4X flash, and NAND/NOR flash interfaces. Functional safety and security requirements are supported with memory error correction and in-line cryptography. The S32N55 is complemented with NXP’s system power management and vehicle networking devices as the S32 Coreride platform’s central vehicle controller solution to accelerate customer designs. The FS04 safe system power management IC combined with NXP’s system power management and vehicle controllers that can consolidate dozens of electronic control units (ECUs) in software-defined vehicles (SDVs).

**Debug engine for S32N55**

PLS Programmierbare Logik & Systeme (Germany) has released the UDE 2024 version of the Universal Debug Engine at the Embedded World 2024. This version supports the multi-core debugging and tracing for the S32N55 vehicle super-integration processor. The processor targets central vehicle controllers that can consolidate dozens of electronic control units (ECUs) in software-defined vehicles (SDVs).
Depending on the software partitioning of the applications running on the processor and the particular debug scenarios, the UDE’s synchronization behavior can be flexibly changed. The integrated run control management allows to define a run control group for partial synchronization, for example, in which only a subset of the cores is synchronized. To control all cores individually, synchronization can also be deactivated. For applications where tasks are distributed across multiple cores and shared code is used, UDE’s multi-core breakpoint feature eases debugging. The multi-core breakpoint is effective regardless of which core is currently executing the specific code.

The UDE also provides developers with a detailed insight into the runtime behavior of the system and enables comprehensive analysis based on the recorded trace data. These include profiling, call graph analysis, and code coverage to verify the quality of software tests.

CAN SIC transceiver

CiA member Novosense has introduced the NCA1462-Q1 transceiver, which provides signal improvement capability (SIC) as standardized in ISO 11898-2:2024 (formerly specified in CiA 601-4). According to the Chinese company, the chip features a high EMC performance. This improves the network robustness and optimizes system costs.

In automotive applications with complex working conditions, harsh electromagnetic interference (EMI) in the environment can be coupled to the transceiver through the cable, which can lead to abnormal transmission and even damage the transceiver. The NCA1462-Q1 transceiver has anti-interference capability. Even in extremely harsh electromagnetic environments, it can still maintain CAN FD communication, laying a solid foundation for a robust communication. On the other hand, EMI within the application system can also radiate externally, thus affecting the transmission of communication signals. The launched transceiver is optimized for EMI based on an innovative patented architecture and tested in accordance with IEC 62228-3, as shown in the figures.

In addition, the CAN SIC transceiver achieves a ±8-kV ESD performance by optimizing the circuit structure and layout area. Additionally, it provides a reliable circuit protection against transient ESD threats during automotive driving, while achieving better device cost performance. With this EMC/ESD performance, the transceiver can help engineers to eliminate common mode choke or TVS tubes from peripheral circuits in some designs. Furthermore, the VIO design as low as 1,8 V can further save the use of LDO or level shifter in the system, helping engineers to reduce overall costs.

The NCA1462-Q1 is available in SOP8 and DFN8 packages and is compatible with other CAN HS (high-speed) and CAN FD transceivers. The transceiver meets AEC-Q100, Grade 1 requirements, supports a wide operating temperature range of -40 °C to +125 °C, and provides over-temperature protection. It supports TXD explicit timeout protection and features remote wake-up in standby mode. Samples of the device are available.